22. (New) The microprocessor as recited in claim 15, wherein the microprocessor is adapted to perform a trace function, which outputs the current location of the microprocessor program counter while the microprocessor executes program instructions, wherein the current location of the microprocessor program counter is specified relative to a trigger event generated by the microprocessor.

23. (New) The microprocessor as recited in claim 15, wherein the state restoration logic comprises a multiplexer, which is coupled to the state machine for receiving a current state of the state machine, and coupled to the backup register for receiving the preceding state of the state machine.

24. (New) The microprocessor as recited in claim 23, wherein the multiplexer selects the current state of the state machine for output when a control signal received by the multiplexor indicates a valid trigger event.

25. (New) The microprocessor as recited in claim 24, wherein the microprocessor generates a valid trigger event upon accessing a breakpoint defined by a specified memory address and/or a specified data value.

26. (New) The microprocessor as recited in claim 24, wherein the multiplexer selects the preceding state of the state machine for output when a control signal received by the multiplexor indicates an invalid trigger event.

27. (New) The microprocessor as recited in claim 26, wherein the microprocessor generates an invalid trigger event upon re-executing a branch instruction after returning from an exception associated with an instruction immediately following the branch instruction.

28. (New) The microprocessor as recited in claim 26, further comprising an output register coupled between the multiplexer and the backup register, wherein the output register is adapted for storing the output selected from the multiplexer and for forwarding the output to the backup register for storage therein.